



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D-1485

Applicant : Yutaka Yoshida
Title : DC-DC CONVERTER
Patent No. : 7,061,213 B2
Date of Patent : June 13, 2006
Serial No. : 10/613,017
Filed : July 7, 2003
Group Art Unit : 2838
Examiner :

*Certificate
JUL 20 2006
of Correction*

Hon. Commissioner of Patents and Trademarks
Washington, D. C. 20231

July 18, 2006

REQUEST FOR ISSUANCE OF CERTIFICATE OF CORRECTION

Sir:

The Letters Patent was issued on June 13, 2006, wherein there are clerical errors as follows:

Please change column 12, line 10, "out ud" to -- out_ud--, Column 15, line 55, "FIG. 12(d)" to -- FIG. 12(d). --, Column 23, line 61, "Verr<Vr6" to -- Verr≤Vr6 --, Column 24, line 3, "PFM" to -- PWM --, and Column 25, line 56, "output-signal" to -- output signal --.

JUL 20 2006

The above errors were made by the Patent Office. Therefore, please issue a Certificate of Correction without fee.

Respectfully submitted,

KANESAKA BERNER & PARTNERS
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by 

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 7,061,213 B2

DATED : June 13, 2006

INVENTOR(S) : Yutaka Yoshida

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Please change column 12, line 10, “out ud” to -- out_ud--,

column 15, line 55, “FIG. 12(d)” to -- FIG. 12(d). --,

column 23, line 61, “Verr<Vr6” to -- Verr≤Vr6 --,

column 24, line 3, “PFM” to -- PWM --, and

column 25, line 56, “output-signal” to -- output signal --.

MAILING ADDRESS OF SENDER:

PATENT NO. 7,061,213 B2

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